74HC132; 74HCT132

Quad 2-input NAND Schmitt trigger

Rev. 8 — 11 March 2024 | Product data sheet

1. General description

The 74HC132; 74HCT132 is a quad 2-input NAND gate with Schmitt-trigger inputs. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}. Schmitt trigger inputs transform slowly changing input signals into sharply defined jitter-free output signals.

2. Features and benefits

- Wide supply voltage range from 2.0 to 6.0 V
- CMOS low power dissipation
- High noise immunity
- Unlimited input rise and fall times
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level B
- Complies with JEDEC standards:
  - JESD8C (2.7 V to 3.6 V)
  - JESD7A (2.0 V to 6.0 V)
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Multiple package options
- Specified from −40 °C to +85 °C and from −40 °C to +125 °C

3. Applications

- Wave and pulse shapers
- Astable multivibrators
- Monostable multivibrators

4. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC132D 74HCT132D	-40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74HC132PW 74HCT132PW	-40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
74HC132BQ	-40 °C to +125 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm	SOT762-1

nexperia

5. Functional diagram

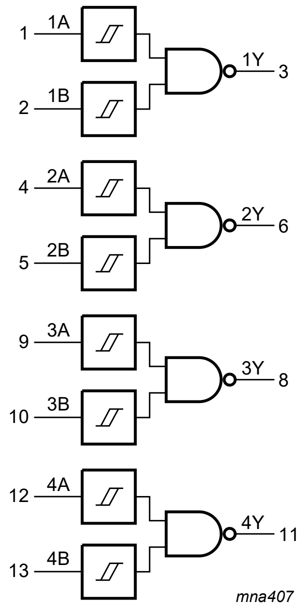


Fig. 1. Logic symbol

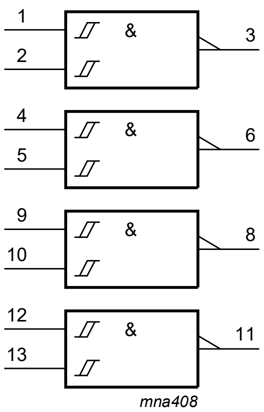


Fig. 2. IEC logic symbol

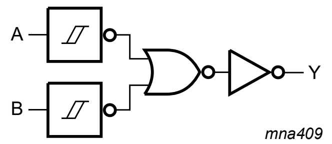
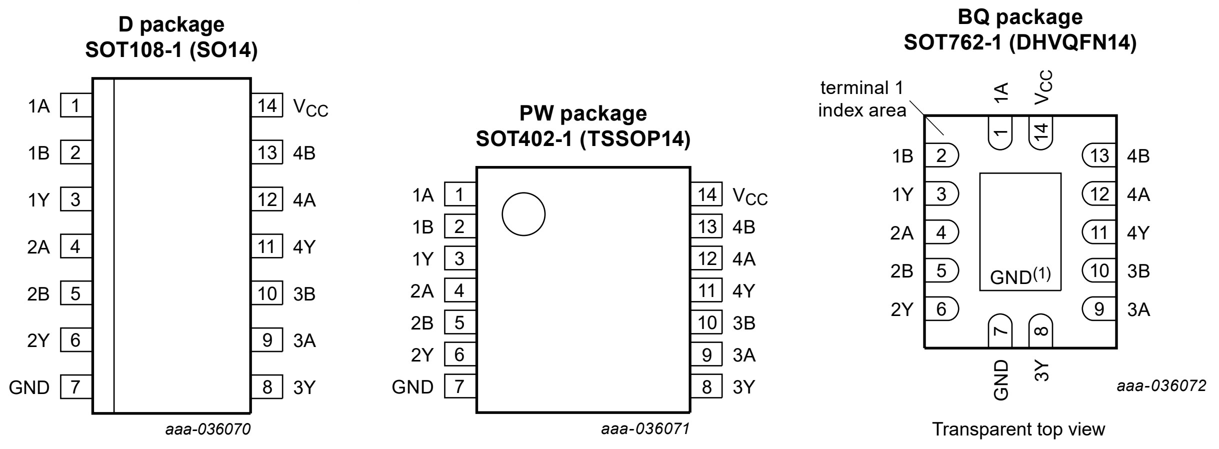


Fig. 3. Logic diagram (one Schmitt trigger)

6. Pinning information

6.1. Pinning



(1) This is not a ground pin. There is no electrical or mechanical requirement to solder the pad. In case soldered, the solder land should remain floating or connected to GND.

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6.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1A, 2A, 3A, 4A	1, 4, 9, 12	data input
1B, 2B, 3B, 4B	2, 5, 10, 13	data input
1Y, 2Y, 3Y, 4Y	3, 6, 8, 11	data output
GND	7	ground (0 V)
V_{CC}	14	supply voltage

7. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level

Input		Output
nA	nB	nY
L	L	H
L	H	H
H	L	H
H	H	L

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			-0.5	+7	V
I_{IK}	input clamping current	$V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V	[1]	-	±20	mA
I_{OK}	output clamping current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V	[1]	-	±20	mA
I_O	output current	-0.5 V $< V_O < V_{CC} + 0.5$ V		-	±25	mA
I_{CC}	supply current			-	50	mA
I_{GND}	ground current			-50	-	mA
T_{stg}	storage temperature			-65	+150	°C
P_{tot}	total power dissipation		[2]	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SOT108-1 (SO14) package: P_{tot} derates linearly with 10.1 mW/K above 100 °C.
For SOT402-1 (TSSOP14) package: P_{tot} derates linearly with 7.3 mW/K above 81 °C.
For SOT762-1 (DHVQFN14) package: P_{tot} derates linearly with 9.6 mW/K above 98 °C.

9. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	74HC132			74HCT132			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V_I	input voltage		0	-	V_{CC}	0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	0	-	V_{CC}	V
T_{amb}	ambient temperature		-40	+25	+125	-40	+25	+125	°C

10. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC132										
V_{OH}	HIGH-level output voltage	$V_I = V_{T+}$ or V_{T-}								
		$I_O = -20\ \mu A$; $V_{CC} = 2.0\ V$	1.9	2.0	-	1.9	-	1.9	-	V
		$I_O = -20\ \mu A$; $V_{CC} = 4.5\ V$	4.4	4.5	-	4.4	-	4.4	-	V
		$I_O = -20\ \mu A$; $V_{CC} = 6.0\ V$	5.9	6.0	-	5.9	-	5.9	-	V
		$I_O = -4.0\ mA$; $V_{CC} = 4.5\ V$	3.98	4.32	-	3.84	-	3.7	-	V
		$I_O = -5.2\ mA$; $V_{CC} = 6.0\ V$	5.48	5.81	-	5.34	-	5.2	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{T+}$ or V_{T-}								
		$I_O = 20\ \mu A$; $V_{CC} = 2.0\ V$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 20\ \mu A$; $V_{CC} = 4.5\ V$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 20\ \mu A$; $V_{CC} = 6.0\ V$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 4.0\ mA$; $V_{CC} = 4.5\ V$	-	0.15	0.26	-	0.33	-	0.4	V
		$I_O = 5.2\ mA$; $V_{CC} = 6.0\ V$	-	0.16	0.26	-	0.33	-	0.4	V
I_I	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 6.0\ V$	-	-	±0.1	-	±1.0	-	±1.0	μA
I_{CC}	supply current	$V_I = V_{CC}$ or GND; $I_O = 0\ A$; $V_{CC} = 6.0\ V$	-	-	2.0	-	20	-	40	μA
C_I	input capacitance		-	3.5	-	-	-	-	-	pF
74HCT132										
V_{OH}	HIGH-level output voltage	$V_I = V_{T+}$ or V_{T-}; $V_{CC} = 4.5\ V$								
		$I_O = -20\ \mu A$	4.4	4.5	-	4.4	-	4.4	-	V
		$I_O = -4.0\ mA$	3.98	4.32	-	3.84	-	3.7	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{T+}$ or V_{T-}; $V_{CC} = 4.5\ V$								
		$I_O = 20\ \mu A$;	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 4.0\ mA$;	-	0.15	0.26	-	0.33	-	0.4	V

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
I_I	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 5.5$ V	-	-	±0.1	-	±1.0	-	±1.0	μA
I_{CC}	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5$ V	-	-	2.0	-	20	-	40	μA
ΔI_{CC}	additional supply current	per input pin; $V_I = V_{CC} - 2.1$ V; other inputs at V_{CC} or GND; $I_O = 0$ A; $V_{CC} = 4.5$ V to 5.5 V	-	30	108	-	135	-	147	μA
C_I	input capacitance		-	3.5	-	-	-	-	-	pF

11. Dynamic characteristics

Table 7. Dynamic characteristics

GND = 0 V; C_L = 50 pF; for test circuit see Fig. 5.

Symbol	Parameter	Conditions	25 °C			−40 °C to +85 °C		−40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC132										
t_{pd}	propagation delay	nA, nB to nY; see Fig. 4 [1]								
		$V_{CC} = 2.0$ V	-	36	125	-	155	-	190	ns
		$V_{CC} = 4.5$ V	-	13	25	-	31	-	38	ns
		$V_{CC} = 5.0$ V; $C_L = 15$ pF	-	11	-	-	-	-	-	ns
		$V_{CC} = 6.0$ V	-	10	21	-	26	-	32	ns
t_t	transition time	see Fig. 4 [2]								
		$V_{CC} = 2.0$ V	-	19	75	-	95	-	110	ns
		$V_{CC} = 4.5$ V	-	7	15	-	19	-	22	ns
		$V_{CC} = 6.0$ V	-	6	13	-	16	-	19	ns
C_{PD}	power dissipation capacitance	per package; V_I = GND to V_{CC} [3]	-	24	-	-	-	-	-	pF
74HCT132										
t_{pd}	propagation delay	nA, nB to nY; see Fig. 4 [1]								
		$V_{CC} = 4.5$ V	-	20	33	-	41	-	50	ns
		$V_{CC} = 5.0$ V; $C_L = 15$ pF	-	17	-	-	-	-	-	ns
t_t	transition time	$V_{CC} = 4.5$ V; see Fig. 4 [2]	-	7	15	-	19	-	22	ns
C_{PD}	power dissipation capacitance	per package; V_I = GND to $V_{CC} - 1.5$ V [3]	-	20	-	-	-	-	-	pF

[1] t_{pd} is the same as t_{PHL} and t_{PLH}.

[2] t_t is the same as t_{THL} and t_{TLH}.

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum (C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

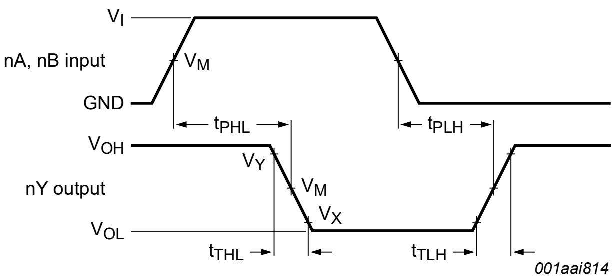
C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

$\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

11.1. Waveforms and test circuit



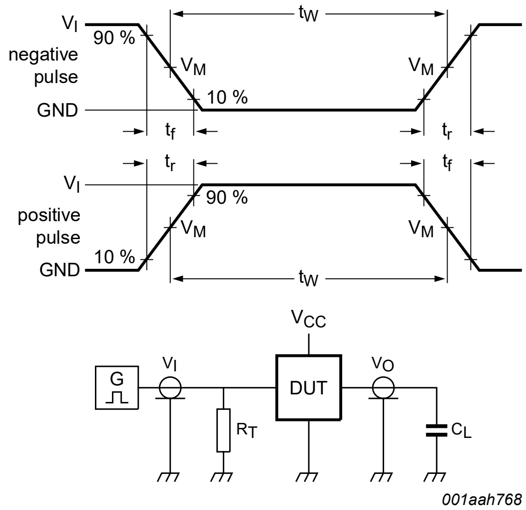
Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 4. Input to output propagation delays

Table 8. Measurement points

Type	Input	Output		
	V_M	V_M	V_X	V_Y
74HC132	$0.5V_{CC}$	$0.5V_{CC}$	$0.1V_{CC}$	$0.9V_{CC}$
74HCT132	1.3 V	1.3 V	$0.1V_{CC}$	$0.9V_{CC}$



Test data is given in Table 9.

Definitions test circuit:

R_T = termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = load capacitance including jig and probe capacitance.

Fig. 5. Test circuit for measuring switching times

Table 9. Test data

Type	Input		Load	Test
	V_I	t_r, t_f	C_L	
74HC132	V_{CC}	6.0 ns	15 pF, 50 pF	t_{PLH}, t_{PHL}
74HCT132	3.0 V	6.0 ns	15 pF, 50 pF	t_{PLH}, t_{PHL}

12. Transfer characteristics

Table 10. Transfer characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); for waveforms see Fig. 6 to Fig. 9.

Symbol	Parameter	Conditions	T_{amb} = 25 °C			T_{amb} = −40 °C to +85 °C		T_{amb} = −40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC132										
V_{T+}	positive-going threshold voltage	V_{CC} = 2.0 V	0.7	1.18	1.5	0.7	1.5	0.7	1.5	V
		V_{CC} = 4.5 V	1.7	2.38	3.15	1.7	3.15	1.7	3.15	V
		V_{CC} = 6.0 V	2.1	3.14	4.2	2.1	4.2	2.1	4.2	V
V_{T-}	negative-going threshold voltage	V_{CC} = 2.0 V	0.3	0.63	1.0	0.3	1.0	0.3	1.0	V
		V_{CC} = 4.5 V	0.9	1.67	2.2	0.9	2.2	0.9	2.2	V
		V_{CC} = 6.0 V	1.2	2.26	3.0	1.2	3.0	1.2	3.0	V
V_H	hysteresis voltage	V_{CC} = 2.0 V	0.2	0.55	1.0	0.2	1.0	0.2	1.0	V
		V_{CC} = 4.5 V	0.4	0.71	1.4	0.4	1.4	0.4	1.4	V
		V_{CC} = 6.0 V	0.6	0.88	1.6	0.6	1.6	0.6	1.6	V
74HCT132										
V_{T+}	positive-going threshold voltage	V_{CC} = 4.5 V	1.2	1.41	1.9	1.2	1.9	1.2	1.9	V
		V_{CC} = 5.5 V	1.4	1.59	2.1	1.4	2.1	1.4	2.1	V
V_{T-}	negative-going threshold voltage	V_{CC} = 4.5 V	0.5	0.85	1.2	0.5	1.2	0.5	1.2	V
		V_{CC} = 5.5 V	0.6	0.99	1.4	0.6	1.4	0.6	1.4	V
V_H	hysteresis voltage	V_{CC} = 4.5 V	0.4	0.56	-	0.4	-	0.4	-	V
		V_{CC} = 5.5 V	0.4	0.60	-	0.4	-	0.4	-	V

12.1. Transfer characteristics waveforms

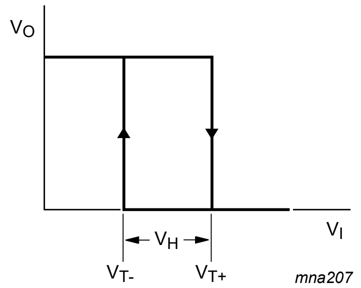


Fig. 6. Transfer characteristics

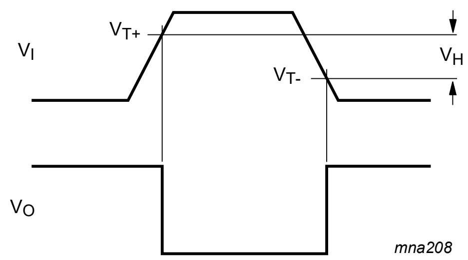
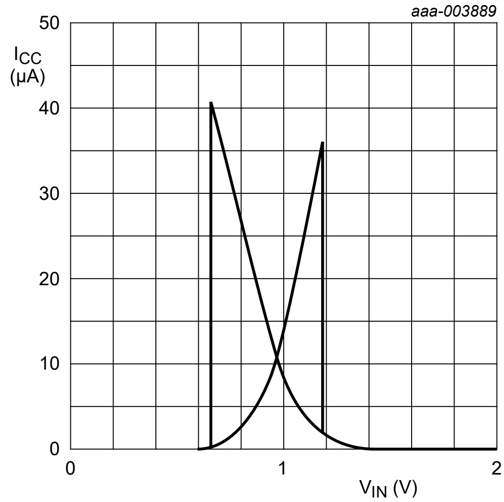
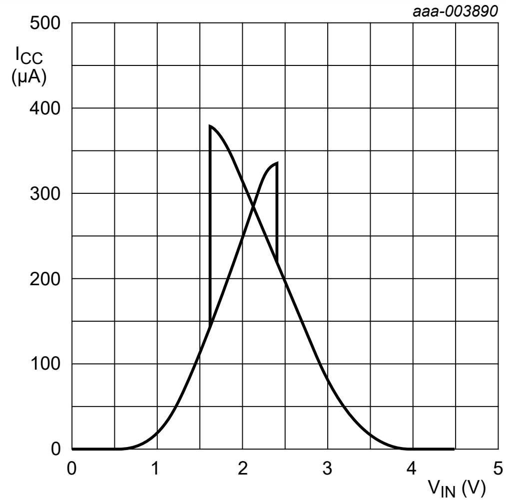


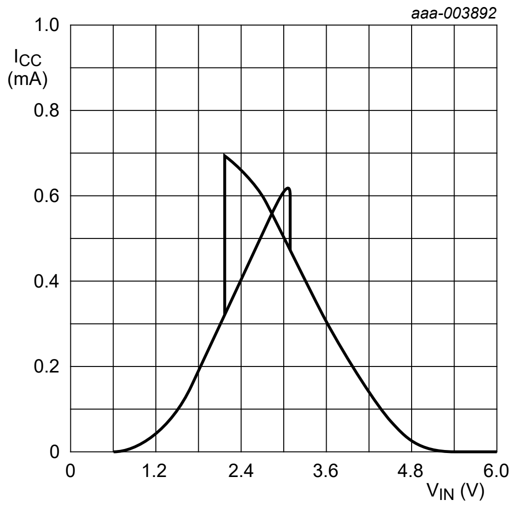
Fig. 7. Transfer characteristics definitions



a. V_{CC} = 2.0 V

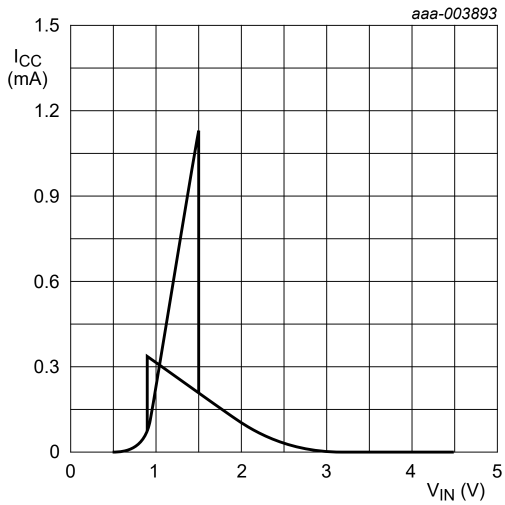


b. V_{CC} = 4.5 V

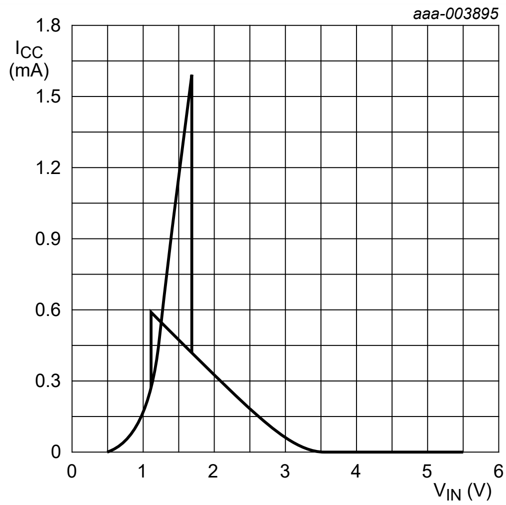


c. V_{CC} = 6.0 V

Fig. 8. Typical 74HC132 transfer characteristics



a. V_{CC} = 4.5 V



b. V_{CC} = 5.5 V

Fig. 9. Typical 74HCT132 transfer characteristics

13. Application information

The slow input rise and fall times cause additional power dissipation, this can be calculated using the following formula:

$P_{add} = f_i \times (t_r \times \Delta I_{CC(AV)} + t_f \times \Delta I_{CC(AV)}) \times V_{CC}$ where:

P_{add} = additional power dissipation (μW);
f_i = input frequency (MHz);
t_r = rise time (ns); 10 % to 90 %;
$\Delta I_{CC(AV)}$ = average additional supply current (μA).
t_f = fall time (ns); 90 % to 10 %;

Average $\Delta I_{CC(AV)}$ differs with positive or negative input transitions, as shown in Fig. 10 and Fig. 11.

An example of a relaxation circuit using the 74HC132; 74HCT132 is shown in Fig. 12.

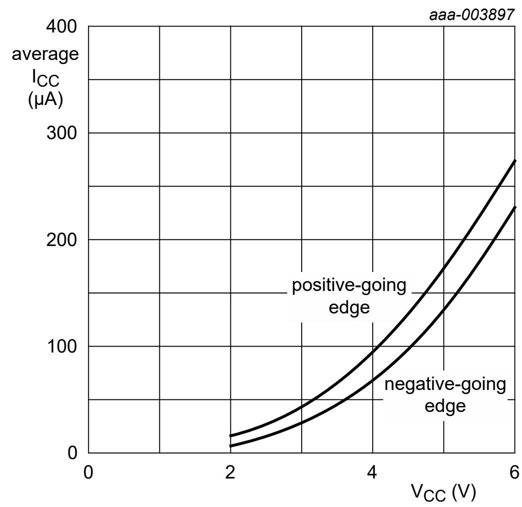


Fig. 10. Average additional supply current as a function of V_{CC} for 74HC132; linear change of V_I between $0.1V_{CC}$ to $0.9V_{CC}$.

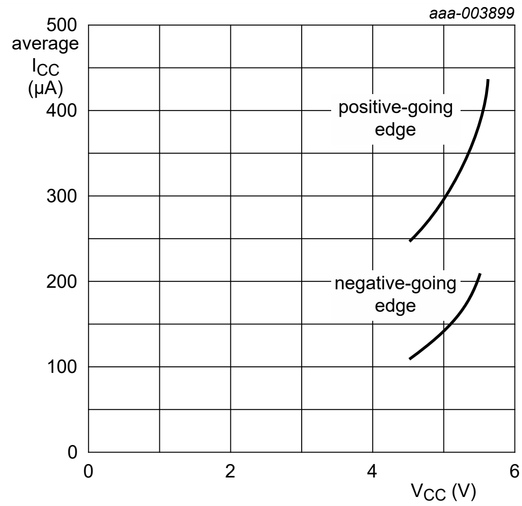
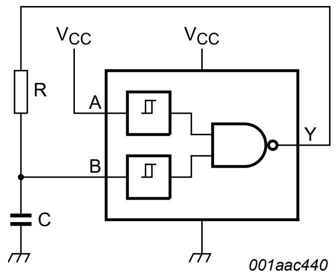


Fig. 11. Average additional supply current as a function of V_{CC} for 74HCT132; linear change of V_I between $0.1V_{CC}$ to $0.9V_{CC}$.



For 74HC132 and 74HCT132: $f = \frac{1}{T} \approx \frac{1}{K \times RC}$

Typical K-factor for relaxation oscillator, see Fig. 13 and Fig. 14

Fig. 12. Relaxation oscillator

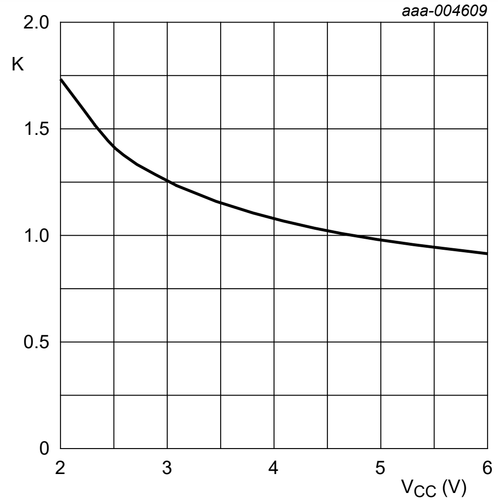


Fig. 13. K-factor for 74HC132

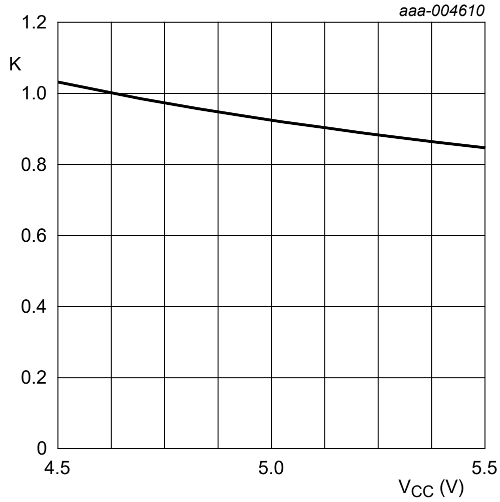
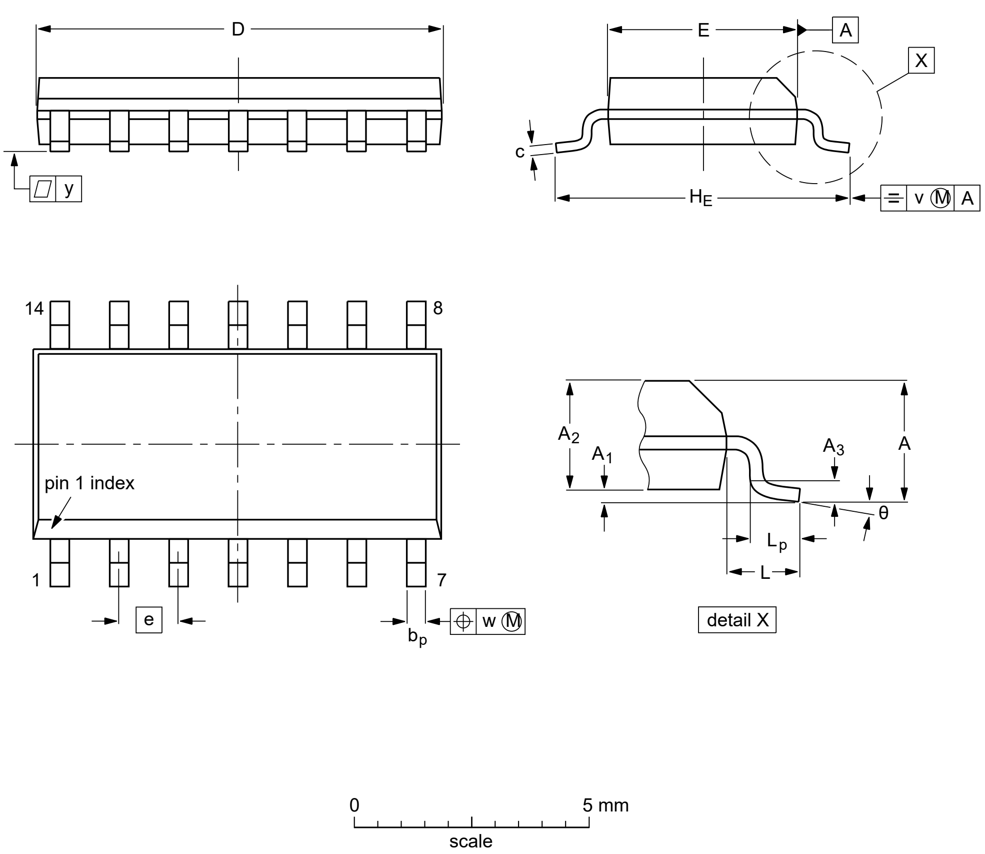


Fig. 14. K-factor for 74HCT132

14. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm **SOT108-1**



Dimensions (inch dimensions are derived from the original mm dimensions)

Unit		A	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	v	w	y	θ
mm	max	1.75	0.25			0.51	0.25	8.75	4.0		6.2		1.27				8°
	nom				0.25					1.27		1.05		0.2	0.25	0.1	
	min		0.10	1.25		0.31	0.10	8.55	3.8		5.8		0.4				0°
inches	max	0.069	0.010			0.020	0.010	0.344	0.16		0.244		0.05				8°
	nom				0.01					0.05		0.041		0.008	0.01	0.004	
	min		0.004	0.049		0.012	0.004	0.337	0.15		0.228		0.016				0°

Note

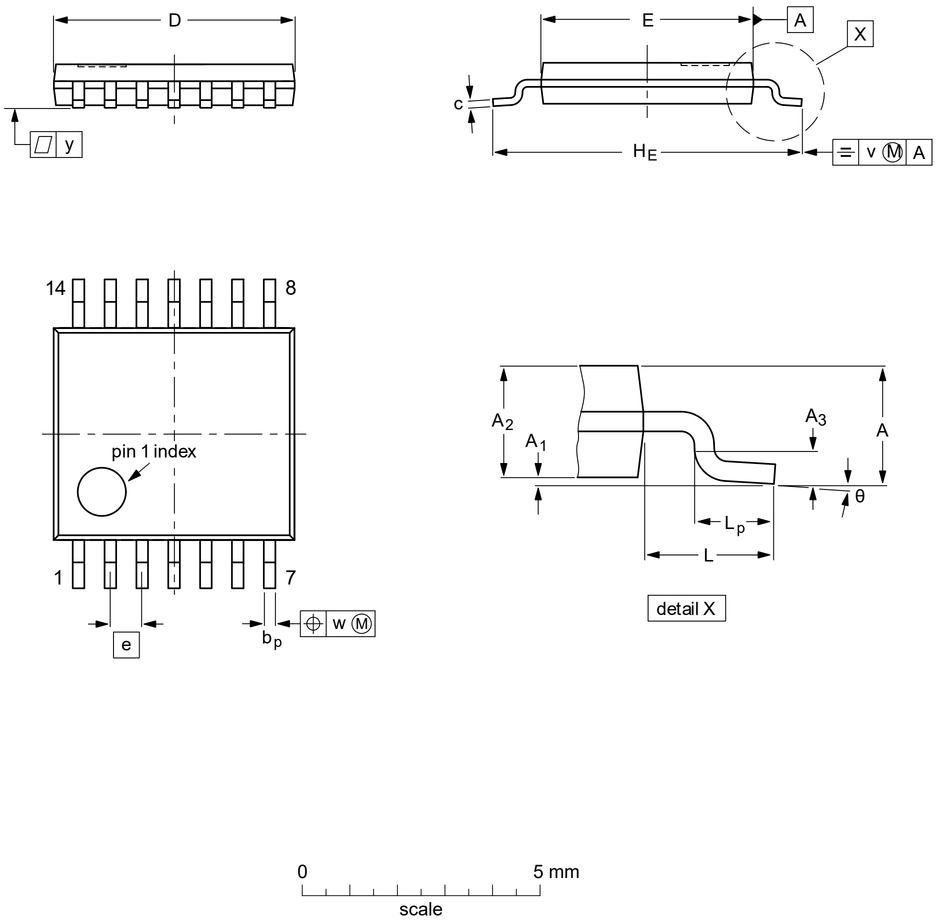
1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

sot108-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT108-1		MS-012				~~03-02-19~~ 23-10-27

Fig. 15. Package outline SOT108-1 (SO14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm **SOT402-1**



Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	v	w	y	θ
mm	max	1.20	0.15	1.05		0.30	0.2	5.1	4.5		6.6		0.75				8°
	nom				0.25					0.65		1		0.2	0.1	0.1	
	min		0.05	0.80		0.19	0.09	4.9	4.3		6.2		0.45				0°

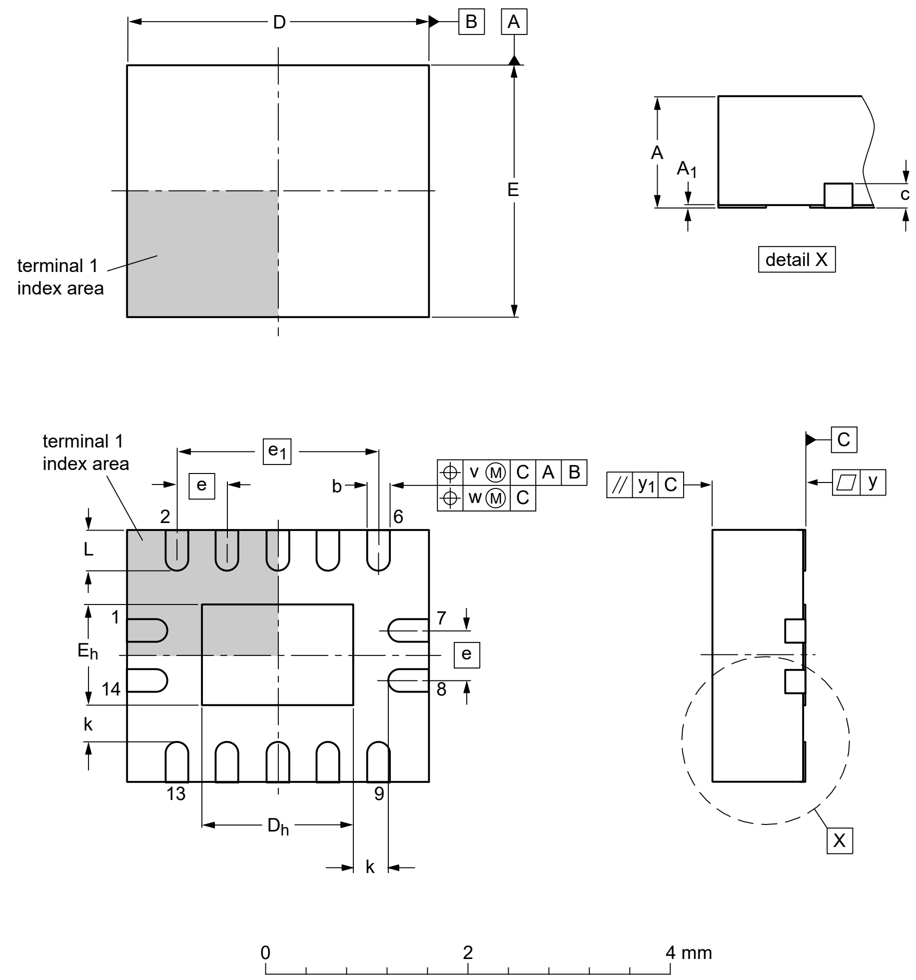
Note
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

sot402-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT402-1		MO-153				~~03-02-18~~ 23-10-27

Fig. 16. Package outline SOT402-1 (TSSOP14)

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm **SOT762-1**



Dimensions (mm are the original dimensions)

Unit		A(1)	A_1	b	c	D(1)	D_h	E(1)	E_h	e	e_1	k	L	v	w	y	y_1
mm	max	1	0.05	0.30		3.1	1.65	2.6	1.15				0.5				
	nom		0.02	0.25	0.2	3.0	1.50	2.5	1.00	0.5	2		0.4	0.1	0.05	0.05	0.1
	min		0.00	0.18		2.9	1.35	2.4	0.85			0.2	0.3				

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot762-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT762-1		MO-241				~~15-04-10~~ 15-05-05

Fig. 17. Package outline SOT762-1 (DHVQFN14)

15. Abbreviations

Table 11. Abbreviations

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model

16. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT132 v.8	20240311	Product data sheet	-	74HC_HCT132 v.7
Modifications:	• Fig. 15, Fig. 16: Aligned SO and TSSOP package outline drawings to JEDEC MS-012 and MO-153. • Section 2: ESD specification updated according to the latest JEDEC standard.			
74HC_HCT132 v.7	20210813	Product data sheet	-	74HC_HCT132 v.6
Modifications:	• Section 2 updated. • Type numbers 74HC132DB and 74HCT132DB (SOT337-1/SSOP16) removed.			
74HC_HCT132 v.6	20190716	Product data sheet	-	74HC_HCT132 v.5
Modifications:	• Type number 74HC132BQ (SOT762-1) added. • Table 4: Derating values for P_{tot} total power dissipation have changed.			
74HC_HCT132 v.5	20180612	Product data sheet	-	74HC_HCT132 v.4
Modifications:	• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate.			
74HC_HCT132 v.4	20151201	Product data sheet	-	74HC_HCT132 v.3
Modifications:	• Type numbers 74HC132N and 74HCT132N (SOT27-1) removed.			
74HC_HCT132 v.3	20120830	Product data sheet	-	74HC_HCT132_CNV v.2
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Fig. 13 and Fig. 14 added (typical K-factor for relaxation oscillator).			
74HC_HCT132_CNV v.2	19970826	Product specification	-	-

17. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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